WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

(a) two or more element forming regions formed on a surface of a semiconductor substrate and defined by an insulating film, said two or more element forming regions each extending in a first direction and being arranged in a second direction perpendicular to said first direction;

(b) a plurality of memory cells formed on main surfaces of said two or more element forming regions; and

(c) a conductive film formed so as to surround said plural memory cells,

wherein said element forming regions extend up to below said conductive film which extends in said second direction.

2. A semiconductor integrated circuit device according to claim 1, wherein each of said memory cells includes:

(a) a first electrode constituted by a first conductive film formed through a first insulating film on any of said element forming regions;

(b) a second electrode constituted by a second conductive film formed through a second insulating film on said first electrode, said second electrode extending in said second direction; and

(c) semiconductor regions formed in the element forming

region on both sides of said second electrode,

and said conductive film comprises said first and second conductive films.

3. A semiconductor integrated circuit device comprising:

(a) an element forming region formed on a surface of a semiconductor substrate and defined by an insulating film, said element forming region having two or more element forming portions each extending in a first direction and arranged in a second direction perpendicular to said first direction, and a connecting portion extending in said second direction to connect end portions of said two or more element forming portions; and

(b) a plurality of memory cells formed on a main surface of said element forming region.

4. A semiconductor integrated circuit device according to claim 3, further comprising:

(c) a conductive film formed so as to surround said plural memory cells,

wherein said connecting portion is formed below said conductive film.

5. A semiconductor integrated circuit device comprising:

(a) three or more element forming regions formed on a surface of a semiconductor substrate and defined by an insulating film, said three or more element forming regions

each extending in a first direction and being arranged in a second direction perpendicular to said first direction; and

(b) a plurality of memory cells formed on main surfaces of said three or more element forming regions,

wherein the width in said second direction of an outermost element forming region out of said three or more element forming regions is larger than the width of each of the other element forming regions.

6. A semiconductor integrated circuit device according to claim 5, further comprising:

(c) a conductive film formed so as to surround said plural memory cells,

wherein said element forming regions extend up to below said conductive film which extends in said second direction.

7. A semiconductor integrated circuit device according to claim 3,

wherein said three or more element forming portions are arranged in said second direction perpendicular to said first direction, and

wherein the width in said second direction of an outermost element forming portion out of said three or more element forming portions is larger than the width of each of the other element forming portions.

8. A semiconductor integrated circuit device according to claim 7, further comprising:

(c) a conductive film formed so as to surround said plural memory cells,

wherein said connecting portion is formed below said conductive film.

9. A semiconductor integrated circuit device comprising:

(a) three or more element forming regions formed on a surface of a semiconductor substrate and defined by an insulating film, said three or more element forming regions each extending in a first direction and being arranged in a second direction perpendicular to said first direction; and

(b) a plurality of memory cells formed on main surfaces of the element forming regions other than an outermost element forming region, out of said three or more element forming regions,

wherein a cell functioning as a memory cell is not formed on said outermost element forming region.

10. A semiconductor integrated circuit device comprising:

(a) three or more element forming regions formed on a surface of a semiconductor substrate and defined by an insulating film, said three or more element forming regions each extending in a first direction and being arranged in a direction perpendicular to said first direction; and

(b) a plurality of memory cells formed on each of said element forming regions, said memory cells each including:

(b_1) a first electrode constituted by a first conductive film formed through a first insulating film;

(b_2) a second electrode constituted by a second conductive film formed through a second insulating film on said first electrode, said second electrode extending in said second direction; and

(b_3) semiconductor regions formed on the element forming region on both sides of said second electrode,

wherein the memory cells formed on an outermost element forming region out of said three or more element forming regions do not function as memory cells.

11. A semiconductor integrated circuit device according to claim 10, further comprising:

(c) wiring lines formed on said memory cells; and

(d) a conductive portion formed on said semiconductor regions of each said memory cell to provide an electrical connection between said wiring lines and the memory cells,

wherein said conductive portion is not formed on said outermost element forming region.

12. A semiconductor integrated circuit device according to claim 10, wherein said second electrodes of said plural memory cells do not extend beyond said outermost element

forming region.

13. A semiconductor integrated circuit device according to claim 10, wherein said second electrodes of said plural memory cells comprise, in an alternately arranged state, one extending beyond said outermost element forming region and the other not extending beyond said outermost element forming region.

14. A semiconductor integrated circuit device according to claim 13, wherein in an end portion of the second electrode not extending beyond said outermost element forming region there is disposed a draw-out portion of the second electrode adjacent thereto.

15. A semiconductor integrated circuit device according to claim 10, further comprising:

(c) a conductive film formed so as to surround said plural memory cells,

wherein said element forming regions extend up to below said conductive film which extends in said second direction.

16. A semiconductor integrated circuit device comprising:

(a) an element forming region formed on a surface of a semiconductor substrate and defined by an insulating film, said element forming region having three or more element forming portions extending in a first direction and

arranged in a second direction perpendicular to said first direction and a connecting portion extending in said second direction to connect end portions of said three or more element forming portions; and

(b) a plurality of memory cells formed on each of said element forming regions, said memory cells each having:

(b_1) a first electrode constituted by a first conductive film formed through a first insulating film;

(b_2) a second electrode constituted by a second conductive film formed through a second insulating film on said first electrode, said second electrode extending in said second direction; and

(b_3) semiconductor regions formed in said element forming region on both sides of said second electrode,

wherein the memory cells formed on an outermost element forming portion out of said three or more element forming portions do not function as memory cells.

17. A semiconductor integrated circuit device according to claim 16, further comprising:

(c) wiring lines formed on said memory cells; and

(d) a conductive portion formed on said semiconductor regions of each said memory cell to provide an electrical connection between said wiring lines and the memory cells,

wherein said conductive portion is not formed on said

outermost element forming region.

18. A semiconductor integrated circuit device according to claim 16,

wherein said second electrodes of said plural memory cells comprise, in an alternately arranged state, one extending beyond said outermost element forming portion and the other not extending beyond said outermost element forming portion, and

wherein in an end portion of the second electrode not extending beyond said outermost element forming portion there is disposed a draw-out portion of the second electrode adjacent thereto.

19. A semiconductor integrated circuit device according to claim 16, further comprising:

(c) a conductive film formed so as to surround said plural memory cells, and

wherein said connecting portion is formed below said conductive film.

20. A semiconductor integrated circuit device according to claim 1, wherein said conductive film is in a floating state.

21. A semiconductor integrated circuit device according to claim 1, further comprising:

another element forming region in which peripheral

circuits are formed, said another element forming region being formed in a periphery of said element forming regions with said memory cells formed thereon,

wherein said insulating film is present between said element forming regions and said another element forming region.

22. A method of manufacturing a semiconductor integrated circuit device, comprising the steps of:

forming an insulating film on a semiconductor substrate with semiconductor elements formed thereon;

forming connecting holes and wiring trenches in said insulating film;

forming a pre-washing protective film on side walls of said connecting holes and said wiring trenches; and

performing pre-washing for said semiconductor substrate and subsequently burying a conductive film in said connecting holes and said wiring trenches.

23. A semiconductor integrated circuit device comprising:

(a) three or more element forming regions formed on a surface of a semiconductor substrate and defined by an insulating film, said three or more element forming regions each extending in a first direction and being arranged in a second direction perpendicular to said first direction;

(b) a plurality of memory cells formed on each of said element forming regions, said memory cells each including:

(b_1) a first electrode constituted by a first conductive film formed through a first insulating film;

(b_2) a second electrode constituted by a second conductive film formed through a second insulating film on said first electrode, said second electrode extending in said second direction; and

(b_3) semiconductor regions formed on the element forming region on both sides of said second electrode,

wherein pseudo memory cells formed on an outermost element forming region out of said three or more element forming regions do not function as memory cells, and

wherein a semiconductor region of said pseudo memory cell is connected with ground potential.

24. A semiconductor integrated circuit device according to claim 23, wherein said second conductive film is in a floating state.

25. A semiconductor integrated circuit device according to claim 23, wherein said semiconductor region of said pseudo memory cells is in an OFF state.

26. A semiconductor integrated circuit device according to claim 23, wherein a connecting portion extending in said second direction is provided to connect end portions of said three or more element forming regions.

27. A semiconductor integrated circuit device according to claim 26, wherein said second conductive film is in a floating state.

28. A semiconductor integrated circuit device according to claim 26, wherein said semiconductor region of said pseudo memory cells is in an OFF state.

29. A semiconductor integrated circuit device according to claim 23, wherein said three or more element forming regions are arranged in said second direction perpendicular to said first direction, and

wherein a width in said second direction of an outermost element forming region out of said three or more element forming regions is larger than a width in said second direction of each of the other element forming regions.

30. A semiconductor integrated circuit device according to claim 29, wherein said second conductive film is in a floating state.

31. A semiconductor integrated circuit device according to claim 29, wherein said semiconductor region of said pseudo memory cells is in an OFF state.